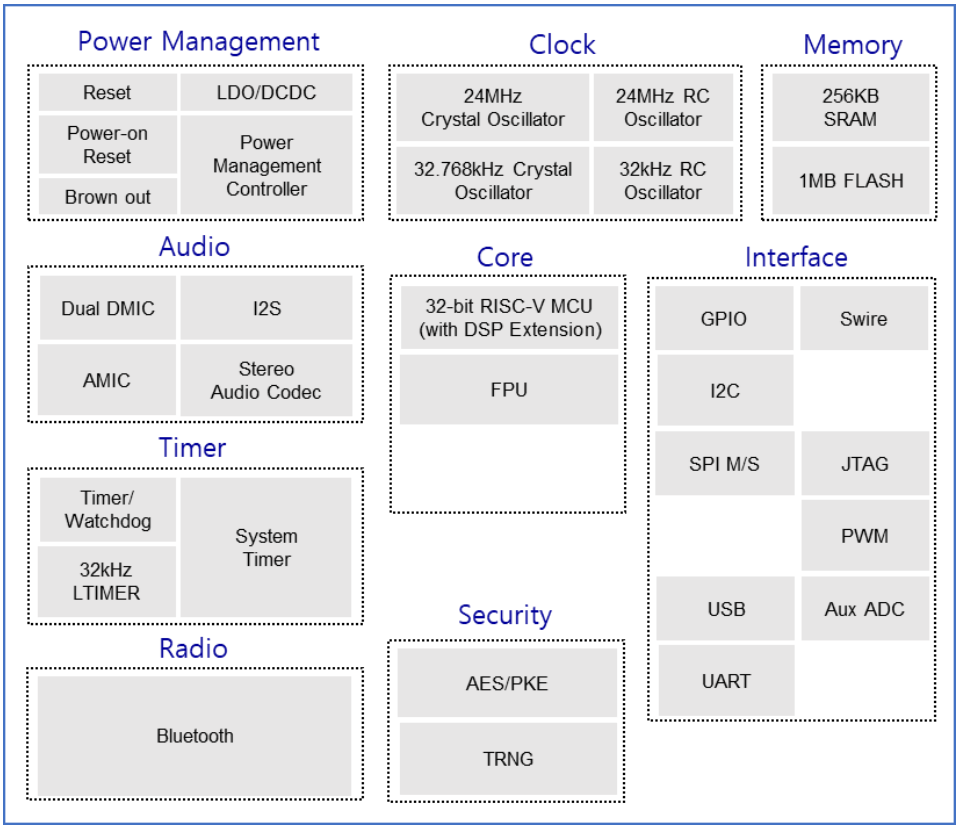
Overview

The TLSR9513 supports standards and industrial alliance specifications including Bluetooth 5.2, Basic data rate (BR), Enhanced data rate (EDR), LE, indoor positioning and BLE Mesh standard. The TLSR9513 combines the features and functions needed for high quality wireless audio equipment into a single SoC. The TLSR9513 is designed to offer high integration, ultra-low power application capabilities.



Applications

- Augmented reality glasses
- Smart watches
- Smart trackers
- Wristband
- Wireless headsets
- Earbuds

Key Features

32-bit RISC-V MCU

- Max.96MHz operating frequency
- 2.59 DMIPS/MHz, 3.54 CoreMark/MHz
- DSP instruction set, floating-point unit

Protocols

- Bluetooth 5.2 compliant
- BLE: 1Mbps/2Mbps/Mesh
- BT Classic: BR 1Mbps/EDR 2Mbps/EDR 3Mbps
- Multi-protocol concurrent mode
- HW OTA upgrade and multiple boot switch

Memory

- Max.256KB SRAM w/ max. 64KB retention
- Program memory: 1MB Flash

Power Consumption (@4.2V DCDC)

- EDR: Rx 5mA, Tx 13mA @ 0 dBm
- BLE: Rx 5mA, Tx 5.5mA @ 0 dBm
- Deep sleep: 0.7uA

RF Specification

- Rx sensitivity (dBm)
  - TLSR9513B/D: -92@BR, -92.5@EDR 2Mbps, -86@EDR 3Mbps, -96@BLE 1Mbps, -92.5@BLE 2Mbps, -99.5@LR 125kbps, -98.5@LR 500kbps
  - TLSR9513A/C: -95.5@BR, -96@EDR 2Mbps, -88.5@EDR 3Mbps, -99@BLE 1Mbps, -96.8@BLE 2Mbps, -103@LR 125kbps, -101@LR 500kbps
- Tx output power (max.)
  - TLSR9513B/D: +10dBm@BR/BLE
+1.5dBm@EDR
  - TLSR9513A/C: +22dBm@BLE
+16dBm@BR/EDR

Audio Features

- High-performance stereo audio codec: 24-bit ADC/DAC, SNR >96dB, max. sampling rate 192kHz
- Patented proprietary technology for TWS and 1+N hearable devices with synchronized playback and balanced power on all devices
- Audio codec: SBC, OPUS, LC3
- Voice codec: G.711, a-Law, u-Law, CVSD, mSBC
- Bluetooth profiles: HFP 1.7, HSP 1.2, A2DP 1.3, AVRCP 1.6, SPP 1.2, PBAP 1.0, ANCS, DIS
- Apple iAP2 protocol
- EDR+BLE dual-mode operation
- Noise suppression and echo cancellation
- Supports packet loss concealment (PLC) for voice Processing

Security

- HW AES and AES-CCM
- HW accelerator for Elliptical curve cryptography (ECC)
- Embedded TRNG

Interface

- Max.15 GPIOs
- Configurable to select 2-wire SDP or 5-wire JTAG debug interface
- Dual DMIC
- AMIC
- I2S
- SPI, I2C, USB 2.0, Swire, UART with hardware flow control
- Max.4 channels of differential PWM
- IR transmitter with DMA
- 2-channel 14-bit auxiliary ADC
- Low-power comparator
- Packet Traffic Arbitrator (PTA) for Wi-Fi co-existence

Supply Voltage

- 1.8V ~ 4.3V

Operating Temperature

- -40℃ ~ +85℃

Package

- TLSR9513A/B/C/D, QFN40, 4x6mm